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Application of FGMOS and QFGMOS Technology for Low Power Design of XOR and XNOR gate

Shweta Singh

PG Student [VLSI], Dept. of ECE, IGDTUW, New Delhi, India

ABSTRACT: In the recent technology the main focus is to reduce the power consumption during the design of analog and digital circuits. The power consumption of analog and digital circuit is $P= CfV^2$, means power is proportional to square of supply voltage. So the voltage reduction will be the best approach to reduce the power consumption. Also due to designing of low power and low voltage circuit portability will increase because we need small battery to supply voltage. In this paper 2 input XOR and XNOR gate simulated using Cadence VIRTUOSO 180 nm technology and their power comparison have been made.

KEYWORDS: CMOS, Low Voltage, FGMOS, QFGMOS, Power Consumption, XOR, XNOR Cadence Virtuoso.

I.INTRODUCTION

In today VLSI system design portable and wireless electronic systems are used widely, the power consumption of these devices should be low. The main design criteria is that CMOS digital circuits have low power dissipation and high speed of operation The total power consumption of CMOS circuit having both dynamic and static power in the active mode. The power dissipation occur due to leakage current in triode region. Dynamic power dissipation includes power dissipation because of charging and discharging of load capacitance, also short circuit power dissipation. Leakage current gives the static power dissipation of CMOS. In any case, the threshold voltage of CMOS transistor goes about as a fundamental hindrance in bringing down of voltage supply after certain utmost. The supply must be in any event equivalent to or more prominent than the threshold of MOS transistors utilized as a part of circuit acknowledgment. A new design technology is required to operate the devices at low supply voltage and have low power consumption during the fast scaling of device dimension. In low voltage design FGMOS is most widely used method because effective threshold voltage can be reduced with the bias voltage. But the FGMOS requires large value of capacitance for threshold voltage programmability means it require large the silicon area. It has low effective transconductance and gain-bandwidth (GB) product. FGMOS also creates dc offset problem due to charge storage property. A new device Quasi FGMOS is used to overcome the limitation of FGMOS. In QFGMOS a large value of resistor is used to connect supply voltage with floating gate. A large valued capacitance is not required means chip area will reduce and having high frequency response.

II.XOR AND XNOR GATE USING CMOS LOGIC

The output of XOR gate is at “high” (1) logic level when the inputs are at different logic levels, which can be either 0 and 1 or 1 and 0. And the output is at “low” (0) logic level when the inputs are at the same logic levels. The XOR gate has unique symbol and truth table . XNOR gate is equal to an XOR gate having inverted output. The truth table of XNOR gate is reciprocal XOR gate.

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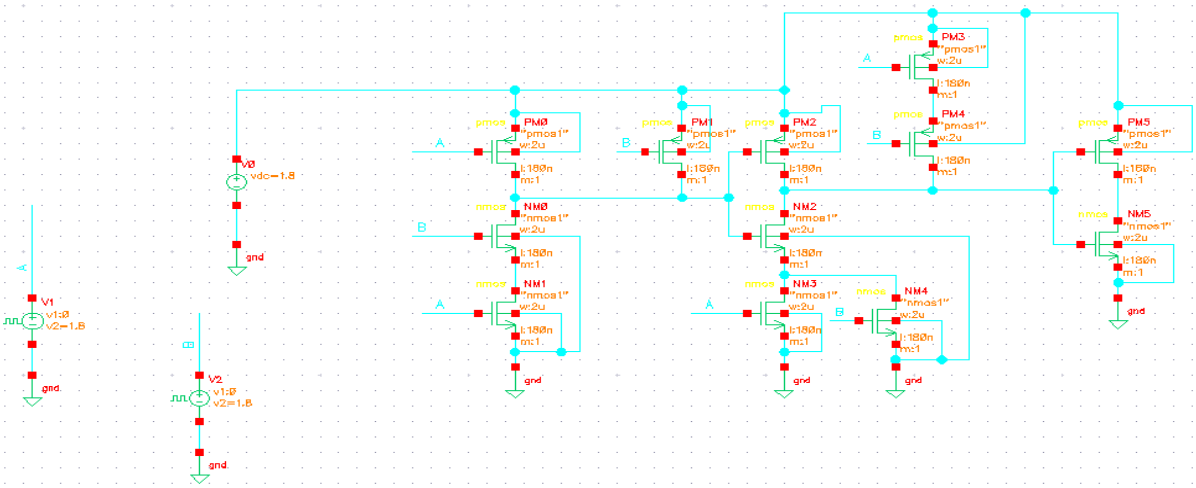

Fig. 1 XOR and XNOR gate using CMOS

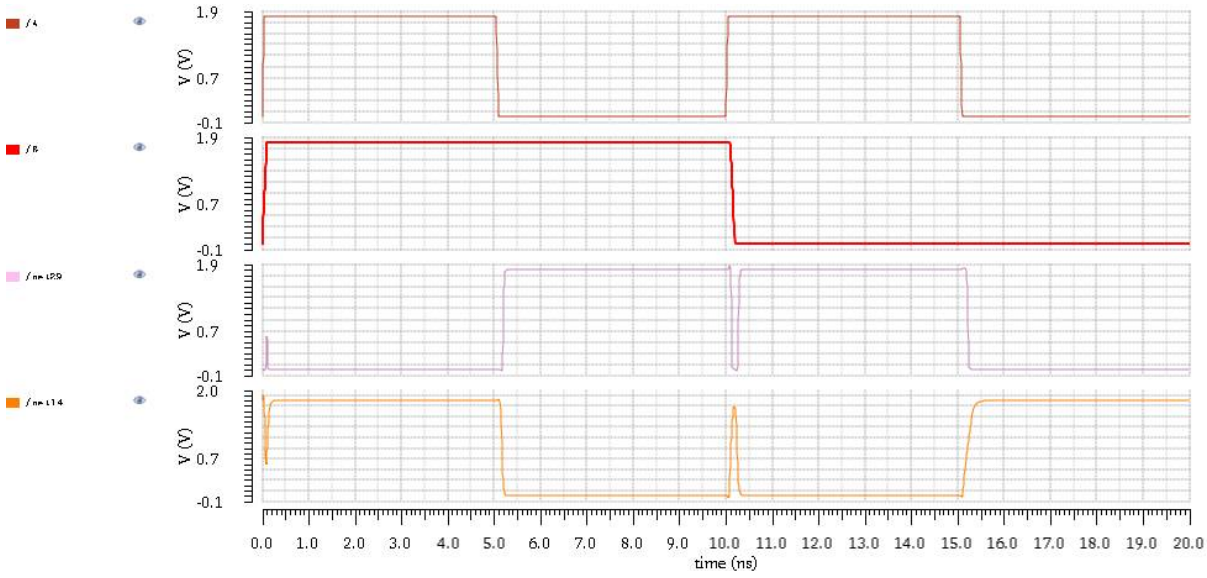

Fig. 2 Output waveform of XOR and XNOR gate

III.FLOATING GATE MOS TRANSISTOR

In 1967 floating gate is firstly introduced and it has non volatile memory. The floating gate transistor used for memory storage application for long period. Now these days in standard CMOS process floating gate transistors are used widely. It has two gates, first is called control gate lying on the top and second gate is isolated called floating gate lying below the control gate . Charge cannot move inside the floating gate without an external force it it is the potential well. Floating gate is the heart of all non volatile memories. It is used independent of external condition in memory cell and changes state from programmed to erased .Threshold voltage of floating gate memory can be calculated as

$$V_T = K - Q_{FG}/ C_{CG}$$

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C_{CG} capacitance between both gates , Q_{FG} floating gate charge and K is constant . By varying floating gate charge threshold voltage is controlled and it can altered from high to low value either by storing or removing charge of floating gate.

A large value of capacitance with various coupling coefficient are connected. V_{FG} is the floating node potential,C1,C2.....Cn is the capacitance and V1,V2.....Vn is the input terminal voltages

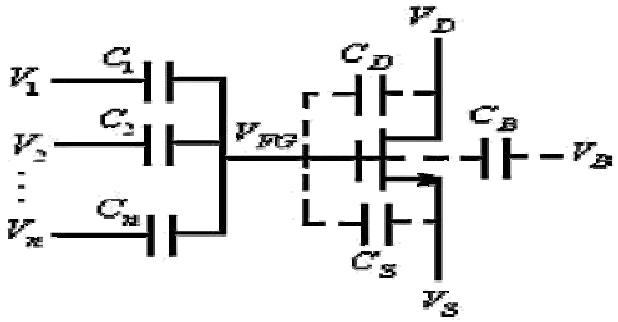

Fig. 3 FGMOS Equivalent circuit

$$Q_{FG} = \sum_{i=1}^{n} Ci\,(V_i - V_{FG}) + (V_S - V_{FG})C_S + (V_D - V_{FG})C_D + (V_G - V_{FG})C_G$$

Q_{FG} charged stored at floating node point, C average capacitance , Cs capacitance between gate and source , C_D is between gate and drain . Q_{FG} should be zero initially.

$$V_{FG} = \frac{\sum_{i=1}^{n} C_i V_i + C_D V_D + C_S V_S + C_G V_G}{\sum_{i=1}^{n} C_i + C_D + C_S + C_G}$$

C_S, C_D and C_B are considered to be negligible as compared to the coupling coefficient.

$$V_{FG} = K_i V_i$$

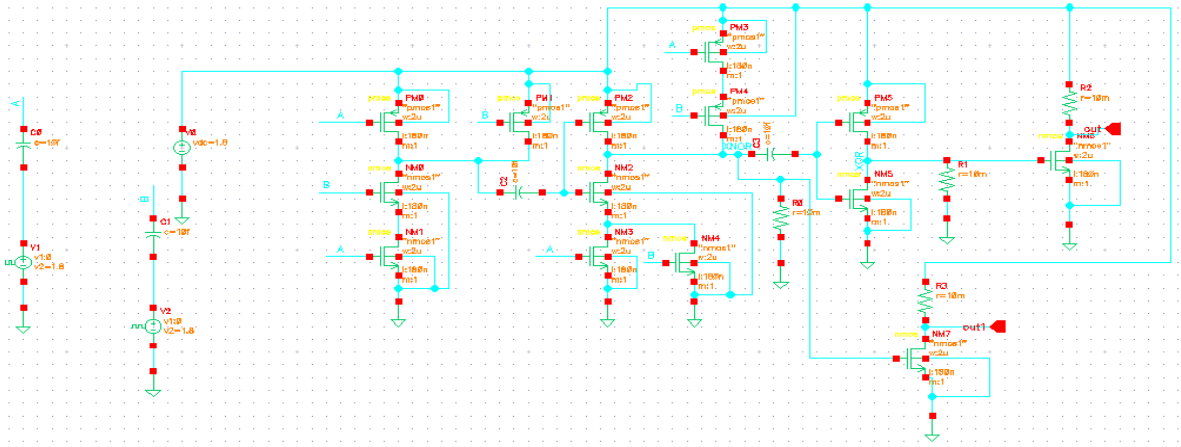

Fig. 4 Schematic of XOR and XNOR gate using FGMOS technology

IV.QUASI FLOATING GATE MOS TRANSISTOR

The Quasi-Floating-Gate MOSFET has same function FGMOS. Both transistors uses capacitor to form voltage dividers and the input voltage is coupled to the gate of the transistor. In FGMOS the DC biasing point is also floating in

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nature. This can cause various issues, for example, the need for programming the limit voltage and Floating gate charge . Both structure have number of voltage input dividers at the gate of MOS transistor. But the difference between them is that QFG having a hig value of resistor connected at the input terminal with the capacitor. Both resistor and capacitor form the parallel RC network at the floating gate of QFGMOS. High value f resistance is created by using diode connected load MOS structure. For NMOS (PMOS) transistor, the gate is connected to the drain terminal. Due to use of large value of resistance supply voltage requirement will reduce. Input stage of a CMOS Op-Amp using QFG transistors operate in the saturation mode with low-voltage supply. Fig. 5(a) shows a 2-input physical layout design of a P-type QFG MOS and Fig. 5(b) shows its equivalent circuit representation of an N-input PMOS QFG transistor .

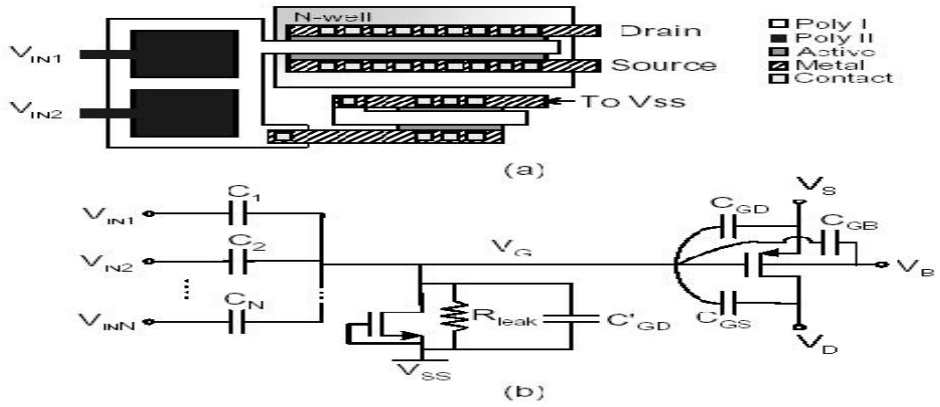

Fig. 5(a): 2-input physical layout design of a P-type QFG transistor and (b) its equivalent circuit of an N-input PMOS QFG transistor.

The voltage appeared at the gate of the QFG transistor is calculated by the measuring the input capacitance voltages and also the parasitic capacitances appeared in MOS transistor. It forms voltage divider with the leakage resistance Rleak and the total capacitance, C_T and it depend on the frequency.

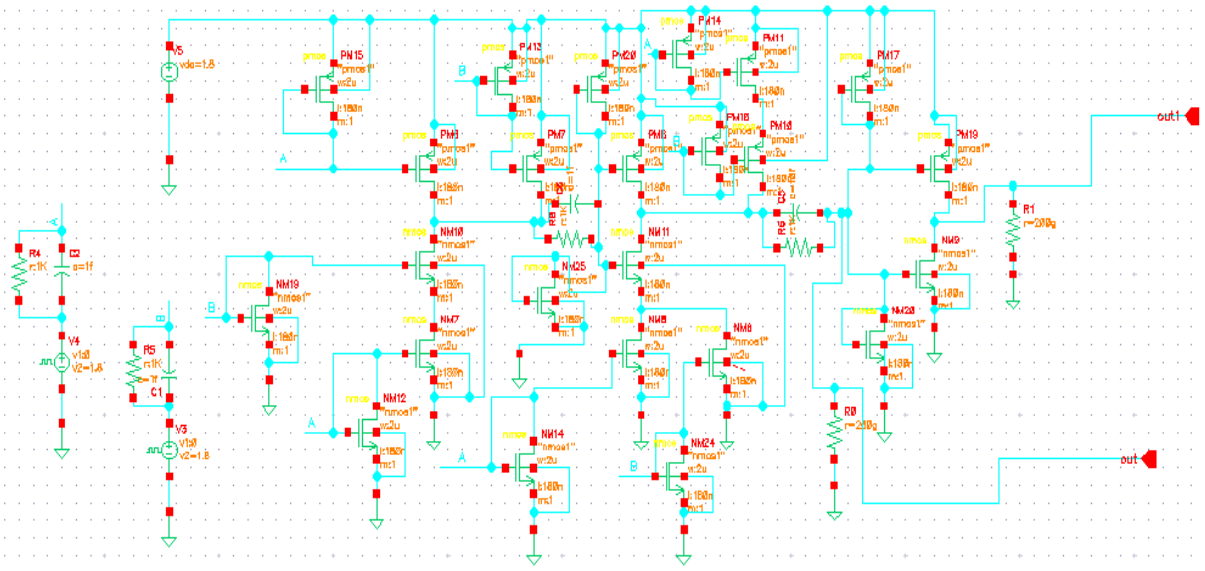

Fig. 6 Schematic of XOR and XNOR gate using QFGMOS technology

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V.SIMULATION RESULT

The FGMOS and QGMOS is simulated using Cadence virtuoso tool under 180nm technology parameters.

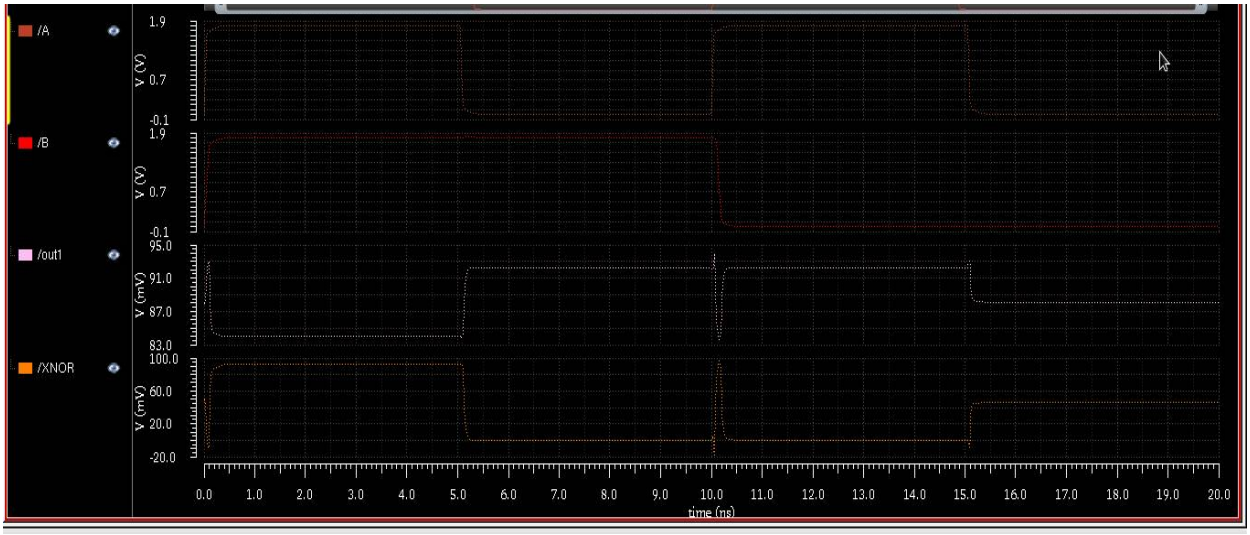

Fig. 7 Transient Analysis of XOR and XNOR gate using FGMOS

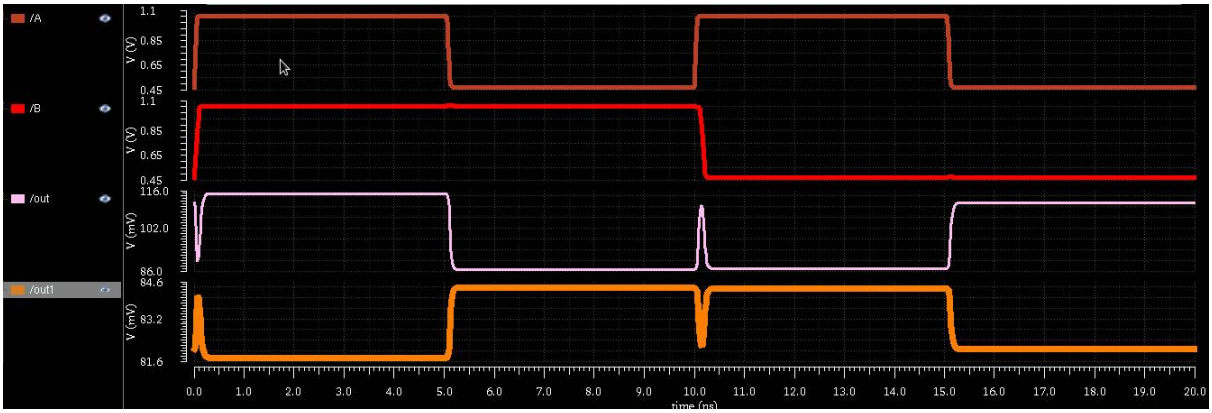

Fig. 8 Transient Analysis of XOR and XNOR gate using QFGMOS

Table1. Comparison of XOR and XNOR gate with FGMOS and QGMOS technique

	XOR and XNOR gate using FGMOS	XOR and XNOR gate using QFGMOS
Technology	180nm	180nm
Power Consumption	1.126mW	4.564mW
Propagation Delay	0.10nsec	0.22nsec

VI.CONCLUSION

In this paper XOR and XNOR gate is simulated using FGMOS and QFGMOS technology to reduce the power consumption. The power dissipation is 1.126mW in case of FGMOS technology which is less as compared to the

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QFGMOS. Also Power delay is less in FGMOS technique. From Table 1. It can be concluded that FGMOS technique can be used in designing of low power and low voltage circuit design.

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